REMARKS

The final Office Action mailed June 3, 2004 and the references cited therein have been carefully considered. Claims 15, 16, 45, and 46 have been amended in a sincere effort to further clarify that which Applicant regards as the invention. Support for this amendment is found generally within the specification, claims, and drawings, as originally filed. Specifically, support for the amendments to Claims 15, 16, 45, and 46 is provided at page 4, lines 18-23, and page 8, lines 25-29 of the specification.

Applicant would like to take this opportunity to thank the Examiner for conducting a telephonic interview with the undersigned on June 9, 2004. During the interview, amendments to the claims, which are submitted herewith, were suggested by the Examiner to further clarify the subject matter recited therein. In addition, arguments submitted during the interview to further clarify distinctions between the claimed invention and the cited references were favorably received by the Examiner and are also set forth herein.

Claims 15-30 and 45-60 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Publication No. 2002/0111699 to Melli et al. (*Melli*) in view of U.S. Patent No. 6,625,592 to Dyer et al. (*Dyer*). Specifically, with respect to Claims 15, 16, 45, and 46, the Office Action states that *Melli* discloses each of the recited elements, except for transferring substantially simultaneously the table in parallel from table memory to operational plane memory in the integrated circuit and outputting a result of the search function. However, it is indicated that *Dyer* teaches these elements at column 5, lines 4-46.

The present invention is directed to a method of performing a search function in an integrated circuit, which includes the steps of storing a table in a table memory in the integrated circuit, inputting a search key, and transferring simultaneously the table in parallel in one instructional cycle from the table memory to an operational plane memory, which is distinct from the table memory, in the integrated circuit. The method also includes performing at least one search function on the table in the operational plane memory using a

search key, and outputting a result of the search function from the integrated circuit, as now defined by amended Claim 15.

The present invention is also directed to a method of performing a search function in an integrated circuit, which includes the steps of storing a plurality of tables in a table memory in the integrated circuit, inputting a table identifier, and inputting a search key. The method also includes transferring simultaneously at least one of the plurality of tables represented by the table identifier in parallel in one instructional cycle from the table memory to an operational plane memory, which is distinct from the table memory, in the integrated circuit, performing at least one search function on the at least one table in the operational plane memory using the search key, and outputting result of the search function from the integrated circuit, as now defined by amended Claim 16.

The present invention is further directed to a method of performing a search function, which includes the steps of inputting an unsorted entry, and performing a hash function on the unsorted entries, wherein the hash function arranges the unsorted entries into a sorted table. The method further includes storing the sorted table in a table memory in an integrated circuit, inputting a search key, and transferring simultaneously the sorted table in parallel in one instructional cycle from the table memory to an operational plane, which is distinct from the table memory, in the integrated circuit. The method also includes performing at least one search function on the sorted table in the operational plane memory using the search key, and outputting the result of the search function from the integrated circuit, as now defined by amended Claim 45.

The present invention is yet further directed to a method of performing a search function, which includes the steps of inputting unsorted entries, and performing a first hash function on the unsorted entries, wherein the first hash function arranges the unsorted entries into a plurality of sorted tables. The method also includes storing the plurality of sorted tables in a table memory in an integrated circuit, inputting a search key, and performing a second hash function on the search key, wherein the second hash function outputs a table

identifier representative of one of the plurality of sorted tables in which the search key is likely to be found. The method further includes transferring simultaneously at least one of the plurality of tables represented by the table identifier in parallel in one instruction cycle from the table memory to an operational plane memory, which is distinct from the table memory, in the integrated circuit, performing at least one search function on the at least one table in the operational plane memory using the search key, and outputting a result of the search function from the integrated circuit, as now defined by amended Claim 46.

Melli relates to a method and system for creating and using a generic container as a data structure in a software program. A selected data structure is specified at startup or run-time using a mapping table that tracks specified data structures for each generic container used by the program. Each data structure is abstracted to a generic interface for use with the container. The program interacts with the generic container using the generic interface, which allows the container to add, delete, and lookup data stored in the container, as well as to retrieve a key used by the container. The program uses an object factory to create an instance of a generic container having the generic interface.

At run-time, the object factory refers to the mapping table to determine which data structure is used for each generic container, as described at page 1, paragraphs 5, 12, and 13. However, nothing in *Melli* would teach or suggest performing a search on a table located in a separate area (operational plane memory) from that in which it was originally stored (table memory) in the same integrated circuit, as now defined by amended Claims 15, 16, 45 , and 46. In addition, as the Examiner concedes, *Melli* does not teach the simultaneous transfer of the table from operational plane memory to table memory in parallel in one instruction cycle, as now defined by amended Claims 15, 16, 45, and 46.

Dyer relates to a system, method, and data structure delineated for use in data storage and retrieval. Records stored in shared memory contain data entries and associated hash codes computed from a predetermined hash function. The search request uses the same hash function to generate user codes. The records are searched to find one with hash codes that

equal the user codes. This search involves comparisons of native data type entries that are intended to be faster than character string comparisons. After a record is identified with hash codes matching the user codes, a more comprehensive comparison is made between the selected record and respective data entries of the search request, as described at column 3, line 8 through column 4, line 61.

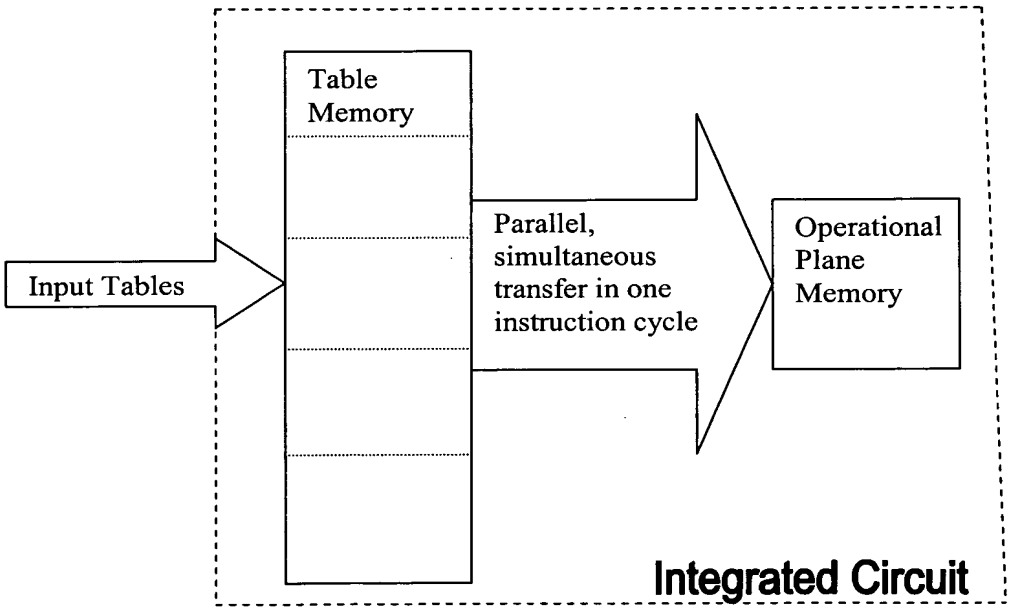


Figure 1

A block diagram of the claimed invention is shown in Figure 1 above. It is respectfully submitted that neither *Melli* nor *Dyer* teach or suggest, either alone or in combination, an integrated circuit that includes table memory, in which a plurality of tables can initially be stored, and operational plane memory, to which at least one table is simultaneously transferred in parallel in one instruction cycle prior to performing a search function therein. Further, neither of the cited references even remotely suggests integrating these functions on the same chip.

The advantage provided by such a configuration in an integrated circuit is that a multitude of tables can be downloaded to the integrated circuit at one time, after which the integrated circuit becomes a self-contained, extremely portable unit capable of providing information from many databases. In addition, the simultaneous transfer of a particular desired table from table memory to a different area (operational plane memory) enables the efficient manipulation of table entries without the potential for corrupting entries in table memory (which can then be kept as an accurate reference) as well as allowing table memory to be accessible to other processes during operation of the search function in operational plane memory.

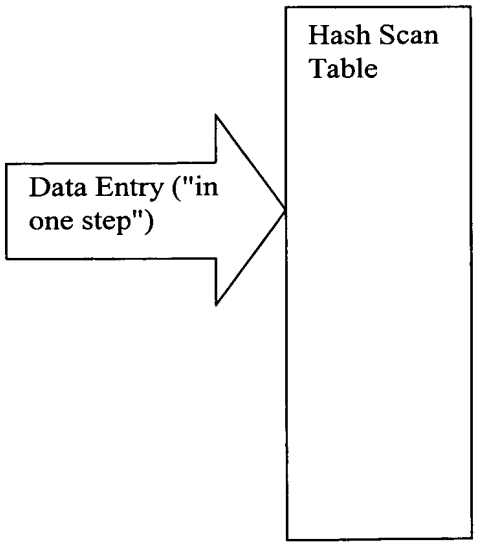


Figure 2

Likewise, the method described in *Dyer* merely enters data into a hash scan table as shown in Figure 2 above. The search is performed in the same area (hash scan table) and thus there is not even a need to simultaneously transfer the contents of the hash scan table in parallel to another area to perform the search function.

Dyer states, at column 5, lines 14-16, that "all data entries are input in a single step 26, and then sequentially processed for hash code generation in step 28". However, it is respectfully submitted that this "single step" merely refers to data entry in step 26 and not to hash code generation in step 28, which is explicitly disclosed as occurring in a sequential fashion for each data entry. In addition, Applicant fails to understand where this "single step" is used to describe transfers to other computers or linked memories in *Dryer*. Further, the "single step" refers only to entering all data and then proceeding to the next step, which it is submitted would not lead one skilled in the art to simultaneously transfer a table in parallel from table memory to operational plane memory in one instruction cycle, as now recited by Claims 15, 16, 45, and 46.

Regarding the motivation to combine *Dyer* and *Melli*, it is respectfully submitted that column 2, lines 7-49 of *Dyer* merely discuss the advantages of hash-based searching as compared to linked-list searching, which would not by itself motivate one skilled in the art to combine the dynamically configurable generic containers in described in *Melli* with hash scanning of shared memory described in *Dyer*. Even if these concepts were combined the claimed invention recited in Claims 15, 16, 45, and 46 would not be arrived at.

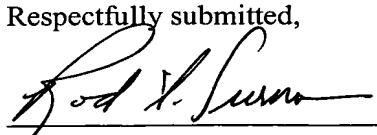
In addition, *Dyer* states at column 7, lines 15-17 that use of shared memory is the fastest way to share data between processes, since the data does not have to be copied between a server process and a client process. If the server process were equated to table memory and the client process were equated to operational plane memory, it is submitted that *Dyer* would clearly teach away from using separate table and operational plane memories in favor of a single shared memory being accessed by multiple processes, which is an entirely different approach than that defined by Claims .15, 16, 45, and 46.

Applicant respectfully notes that in order to support a claim of *prima facie* obviousness, the cited references must teach or suggest each and every element of the invention, and there must be a motivation in the references or the prior art to combine the

references and the prior art as suggested. However, nothing in the art of record, which includes U.S. Publication No. 2002/0118682 to Choe; U.S. Patent No. 5,539,373 to Guha; and U.S. Patent No. 6,157,955 to Narad et al., would teach or suggest, either alone or in combination, a method of performing a search function in an integrated circuit, which includes transferring simultaneously a table in parallel in one instructional cycle from table memory to operational plane memory in the integrated circuit, performing at least one search function on the table in operational plane memory using a search key, and outputting a result of the search function, as now defined by amended Claims 15, 16, 45, and 46.

Applicant respectfully submits that Claims 17-30, which ultimately depend from Claim 16, and Claims 47-60, which ultimately depend from Claim 46 are patentable over the art of record by virtue of their dependency from Claims 1 and 46, respectfully. Further, Applicant submits that Claims 17-30 and 47-60 define patentable subject matter in their own right. Therefore, it is respectfully requested that the rejection of Claims 15-30 and 45-60 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

Respectfully submitted,



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